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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,295	02/23/2004	Chia-Liang Chiang	REAP0015USA	2294
27765	7590	05/12/2005	EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)			LE, DON P	
P.O. BOX 506			ART UNIT	
MERRIFIELD, VA 22116			PAPER NUMBER	
			2819	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/708,295

Applicant(s)

CHIANG, CHIA-LIANG

Examiner

Don P. Le

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 March 2004.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 10-18 is/are allowed.  
6) ☒ Claim(s) 1 and 4-9 is/are rejected.  
7) ☒ Claim(s) 2, 3 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

***Claim Rejections - 35 USC § 102***

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1 and 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Maley et al. (US 5,969,542).

2. With respect to claim 1, figure 2 of Maley discloses a low-to-high level shifter operating under a first supply voltage (VDDIO), the low-to-high level shifter comprising:

a pull-down circuit (N1, N2) coupled to an input signal (IN), the input signal corresponding to a second supply voltage (VDD);

a pull-up circuit (P1, P2) coupled to the pull-down circuit; and

a clamping circuit (N3, N4) coupled to the pull-down circuit, for clamping an operating voltage of the pull-down circuit;

wherein the low-to-high level shifter generates an output signal according to the input signal, the output signal corresponds to the first supply voltage, and the first supply voltage is larger than the second supply voltage.

3. With respect to claim 4, figure 2 of Maley teaches the pull-down circuit comprises a first pull-down transistor (N1) and a second pull-down transistor (N2), control terminals of the first and the second pull-down transistors are coupled to the input signal (IN).

Art Unit: 2819

4. With respect to claim 5, figure 2 of Maley discloses the pull-up circuit comprises a first pull-up transistor (P1) and a second pull-up transistor (P2), a control terminal of the first pull-up transistor is coupled to a first terminal of the second pull-up transistor, and a control terminal of the second pull-up transistor is coupled to a first terminal of the first pull-up transistor.

5. With respect to claim 6, figure 2 of Maley discloses the output signal is extracted first pull-up transistor.

6. With respect to claim 7, figure 2 of Maley discloses the first terminal of the first terminals of the first and the second pull-up transistors are coupled to the pull-down circuit.

7. With respect to claim 8, figure 2 of Maley discloses the clamping circuit comprises a first clamping transistor (N3) and a second clamping transistor (N4), control terminals of the first and the second clamping transistors are coupled to a bias voltage (VREF22).

8. With respect to claim 9, figure 2 of Maley discloses the input signal is coupled to the pull-down circuit via an inverter (I1) operating under the second supply voltage.

***Allowable Subject Matter***

9. Claims 10-18 are allowed

10. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is an examiner's statement of reasons for allowance:

With respect to claims 2 and 10, the prior art does not teach low and high voltage devices.

Art Unit: 2819

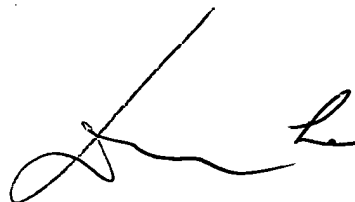
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/6/2005

A handwritten signature in black ink, appearing to read 'Don P. Le', with a stylized flourish at the end.

**DON LE**  
**PRIMARY EXAMINER**